Sensitivity analysis of ramp response of VLSI interconnects.

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***Abstract*—The paper presents the sensitivity analysis of closed form formula for step response of on-chip VLSI interconnect. The formula is calculated with Multiple Scales method and the sensitivity of the method is analyzed and compared with the sensitivity of exact simulation of the interconnect.**

I. Introduction

One of the most important task in VLSI models analysis is the interconnections modelling and simulation. Typical simulation problems consider simulation of the one interconnect or more coupled interconnects. Modern interconnects technology causes growth device speeds and decreasing the wire size. Although long high level interconnects (clock and signal wires) does not scaling so fast. Especially global and clock wires could be 2-8x the minimum dimensions [1]. They have small resistance and high inductance. That gives the condition which distinguish the long interconnections [1]:

$$\frac{R_t}{2Z_0} < 1$$

The resistance of the input gate does not exceed the total interconnect resistance [1] and those condition causes that the output response gives overshoot in first traveling wave. Than the method to calculate such response cannot base on RC transmission line behavior but must takes into account the inductance influence. When the resistance is small compared to inductance of the line, the output response is more like lossless line than RC line. In that work we propose the method based on the lossless line response with some perturbation impact of the losses. The method based on multiple scales method to solve the system of differential equation and is described in further part of the work. The method allows to calculate the closed form formula for the output response both for step and ramp excitation, and then to obtain the closed form for the threshold time formula [2,3]. In that paper we analyze the sensitivity of the ramp response formula and compare it with SPICE simulation sensitivity. In our method there is a possibility to obtain an analytical formula for the sensitivity to the various interconnect parameters.

The paper is organized as follows: in Section II there is presented a step response of high inductance interconnect model calculation using multiple scales method. The method is then extended to ramp response of interconnect. In Section III there is presented sensitivity analysis simulations. The conclusions are presented in the last section.

II. The Method of Calculating Step and Ramp Response of High Inductance Interconnects

Transmission line RLC interconnect model presented in Fig.1. can be described with transmission line equations as follows:

$$\begin{cases} -\dfrac{\partial v}{\partial x} = Ri + L\dfrac{\partial i}{\partial t}, \\ -\dfrac{\partial i}{\partial x} = C\dfrac{\partial v}{\partial t} \end{cases} \tag{1}$$

$$i(x,0) = 0, \quad v(x,0) = 0, \tag{2}$$

$$e(t) - R_s i(0,t) = v(0,t),$$

$$-i(d,t) = C_0 \frac{\partial v(d,t)}{\partial t}, \tag{3}$$

where
R, L, C – line parameters, C_0 – input inverter capacitance, R_s – output inverter resistance, i(x,t), v(x,t) – current and voltage in line, respectively, d – line length, t, x – time and space variable, respectively.

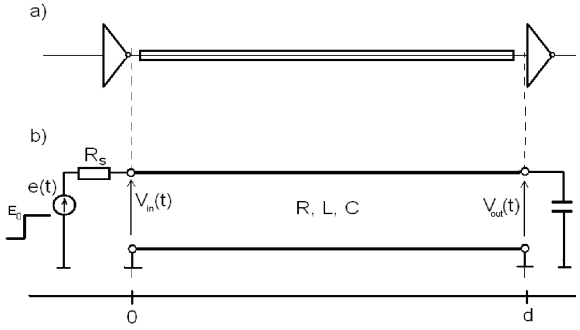

Fig. 1. a) The considered system inverter-interconnect-inverter, b) the model of the considered system

Considering the low-loss line when line resistance R is small compared to lossless line impedance Z0, we can assume that the parameter: $\varepsilon = \dfrac{R_t}{Z_0}$, ($R_t = R \cdot d$) is relatively small and $\varepsilon < 1$. Then we can use the perturbation methods

to solve the system (1). We choose ε as the perturbation parameter and use the multiple scales method [5]. To simplify the calculation and enable the perturbation parameter occur in differential equation we are scaling variables occurring in system (1):

$$y=\frac{x}{d},\ \tau=\frac{t}{\sqrt{L_tC_t}},\ \tilde{v}=-\sqrt{\frac{C_t}{L_t}}v,\ \tilde{e}=\sqrt{\frac{C_t}{L_t}}e,\ \beta=\sqrt{\frac{C_t}{L_t}}R_s$$

and we obtain the new systems of equations in following powers of ε. We consider that systems as consecutively estimations of exact solution

$$\tilde{v}(y,\tau)=\tilde{v}_0(y_0,y_1,\tau)+\varepsilon\cdot\tilde{v}_1(y_0,y_1,\tau),$$
$$i(y,\tau)=i_0(y_0,y_1,\tau)+\varepsilon\cdot i_1(y_0,y_1,\tau),$$
$$y_0=y,\quad y_1=\varepsilon\cdot y.$$

The first approximation for system (1) represents the lossless transmission line model (4):

O(1)

$$-\frac{\partial\tilde{V}_0}{\partial y_0}=sI_0,\qquad -\frac{\partial I_0}{\partial y_0}=s\tilde{V}_0 \tag{4}$$

$$\tilde{E}(\tau)-\beta I_0(0,0,s)=-\tilde{V}_0(0,0,s),\qquad -\alpha I_0(1,\varepsilon,s)=s\tilde{V}_0(1,\varepsilon,s),\qquad \alpha=\frac{C_t}{C_0}, \tag{5}$$

To calculate next O(ε) estimation we need to solve O(1) system and use the solution in second order equation:

O(ε)

$$-\frac{\partial\tilde{V}_1}{\partial y_0}=sI_1+I_0+\frac{\partial\tilde{V}_0}{\partial y_1},\qquad -\frac{\partial I_1}{\partial y_0}=s\tilde{V}_0+\frac{\partial I_0}{\partial y_1} \tag{6}$$

$$-\beta I_1(0,0,s)=-\tilde{V}_1(0,0,s),\qquad -\alpha I_1(1,\varepsilon,s)=s\tilde{V}_1(1,\varepsilon,s) \tag{7}$$

The way of calculating the step output response for such a system is presented in [2]. The output voltage signal for the step response for first traveling way takes the form [2]:

$$v_{out}(d,t)=v_{01}(d,t)+v_{11}(d,t)=$$
$$=\frac{E_0}{\beta+1}\left(A\cdot(t-T)\cdot e^{-\frac{\alpha}{T}(t-T)}-B\cdot\left(1-e^{-\frac{\alpha}{T}(t-T)}\right)\right)\cdot\mathbf{1}(t-T), \tag{8}$$

where $A=-\varepsilon\cdot\alpha\cdot e^{-1.5\varepsilon}$, $B=\frac{\varepsilon}{2}e^{-0.5\varepsilon}\left(1+e^{-\varepsilon}\right)-\frac{\beta\varepsilon}{\beta+1}-2e^{-0.5\varepsilon}$.

Formula (8) is valid for the time 0<t<3T.

Simulation of many on-chip interconnects needs to consider the rise time of input voltage due to the input voltage rise time T_r, is comparable to the time delay of the interconnect. Such excitation can be modeled by the ramp signal. The step response can be easily extended to ramp excitation using relations presented below.

We can express the ramp excitation as

$$v_{in}(t)=\frac{E_0}{T_r}t\cdot 1(t)-\frac{E_0}{T_r}(t-T_r)\cdot 1(t-T_r) \tag{9}$$

We must consider two cases – one for 0<t<T_r, and the other for t>T_r. Denoting the response to ramp excitation at the end of the interconnect as $v^r_{out}(t,d)$ and using

$$v^r_{out}(t,d)=\begin{cases}\int_0^t v_{out}(\tau,d\tau)d\tau & t\le T_r\\ \int_{t-T_r}^t v_{out}(\tau-T_r,d\tau)d\tau & t\ge T_r\end{cases}$$

we have the final output voltage signal

$$v^r_{out}(t)=\frac{E_0}{(\beta+1)T_r}\left[\begin{array}{l}k\left(1-e^{-\alpha\frac{t-T}{T}}\right)\\ -\frac{t-T}{T}\left(B+\frac{A}{\alpha}e^{-\alpha\frac{t-T}{T}}\right)\end{array}\right],\quad for\quad t-T\le T_r$$

$$v^r_{out}(t)=\frac{E_0}{(\beta+1)T_r}\left[\begin{array}{l}\left(\left(\frac{t-T-T_r}{T\alpha}\right)A\right)e^{-\alpha\left(\frac{t-T_r-T}{T}\right)}\\ +k\\ -\left(\frac{t-T}{T\alpha}A+k\right)e^{-\alpha\frac{t-T}{T}}-\frac{T_r}{T}B\end{array}\right],\quad for\quad t-T\ge T_r \tag{10}$$

where $k=\left(\frac{A}{\alpha^2}+\frac{B}{\alpha}\right)$.

The presented approach allows calculating the approximated ramp excitation response. During the simulation we noticed that some improvement could be obtained if the perturbation parameter is scaled to $\varepsilon'=3/5\cdot\varepsilon$. The curve representing the signal calculated using the scaled perturbation parameter is typically almost identical with the curve obtained by the SPICE simulator.

The calculation of threshold crossing time is presented in [2]. The formula for the threshold time can be expressed by:

$$\tau_\rho=\left(1+\frac{K_q-W(z)}{\alpha}\right)\cdot T \tag{11}$$

Where the z and K_q are constant dependent on interconnect parameters and the W(z) function is approximated by:

$$W(z)=\frac{1}{u_1}\ln\left(\frac{z}{u_0}\right)$$

where u_1=-2.988, u_0=-0.887.

Simulations used in investigation of the interconnect response, both the output response and threshold crossing time calculation can be highly sensitive to small changes in the parameter values. Due to generation by the presented approach the closed form formulas for output response (8) and (10), we could calculate the sensitivity of the output response with the formula:

$$S^\lambda_v=\frac{\lambda}{v}\frac{\partial v}{\partial\lambda} \tag{12a}$$

Or for the threshold time:

$$S_{t_\rho}^{\lambda} = \frac{\lambda}{t_\rho}\frac{\partial t_\rho}{\partial \lambda} \qquad (12a)$$

In our work we present the sensitivity of the step response to RLC interconnects parameters and for the output and input gate parameters C_o and R_s respectively. The sensitivity of the formula (10) is compared with the sensitivity of the SPICE simulations. The sensitivity in SPISE program we compute using the output signal with perturbed parameter to which the sensitivity is calculated. We use the following formula to calculate the sensitivity of the ramp response in SPICE:

$$S_{vSPICE}^{\lambda} = \frac{v(t,\lambda) - v(t,\lambda \cdot 1.01)}{v(t,\lambda)} 100 \qquad (13)$$

The similar way we compute the sensitivity of the threshold time for various parameters.

III. Sensitivity Analysis and Simulations

The sensitivity allows to study of how the variation in the output of a model depend on parameters of the model. In our work we consider the low-loss interconnect with high inductance influence, what causes the resistance of the line can be assume as small compared to lossless line impedance. The behavior of such an interconnect allows to analyze only first traveling wave when the information about rise time or threshold time is needed. The exemplary simulation (first traveling wave computed with (10) and compared with SPICE simulation) is presented at Fig.2. The transmission line model parameters are: R_s=25Ω, C_o=0.1pF, R_t=25Ω, L_t=5nF, C_t=1pF, the rise time of the excitation is $\tau_r = T/10$, the parameters are taken from [4].

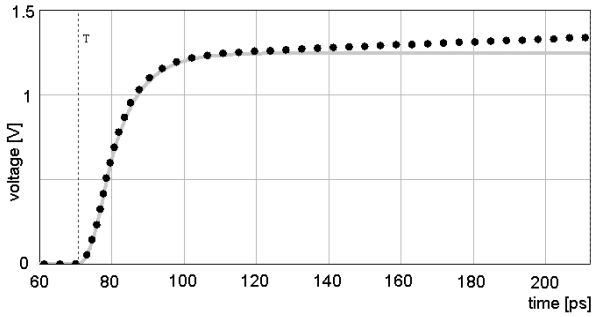

Fig. 2. Ramp response, the solid line presents the sensitivity from Spice simulation, the dots line represents formula (10)

The following simulations presents the sensitivity analysis of the same interconnect as presented in Fig.1. Fig.3. presents the sensitivity of ramp response to the total capacitance of the interconnect in time function. The sensitivity of the method and sensitivity of the SPICE model are almost the same functions. The higher values of sensitivity we can observe during the first period of rise time. The capacitance value changes the delay T value what causes sensitivity in T value equal 100 and decrease with time grows. We can observe that for threshold values exceeded 50% of steady state (0.5V) the sensitivity is less than 10.

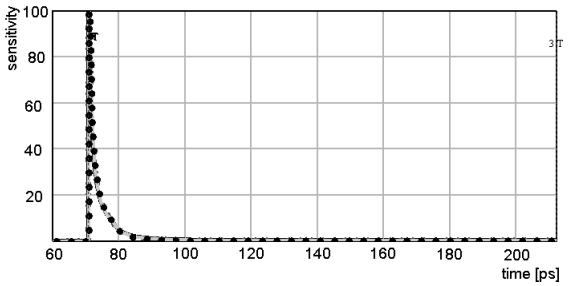

Fig. 3. Sensitivity of the ramp response to the capacitance vs. time function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (10)

The similar behavior as for capacitance changes we can observe for sensitivity to inductance. The simulation result is presented in Fig.4.

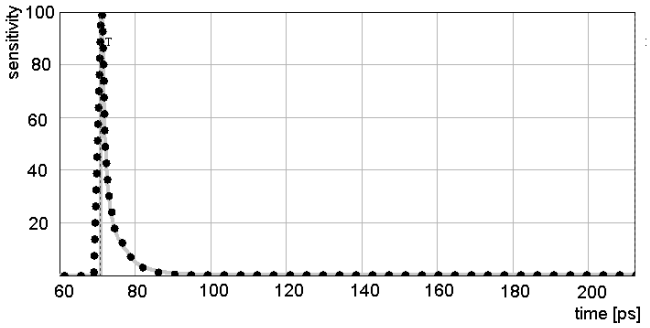

Fig. 4. Sensitivity of the ramp response to the inductance vs. time function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (10)

The following simulation presents the sensitivity to resistance of the interconnect. The sensitivity of the SPICE model and formula (10) considerably changes, but their values does not exceed 0.25. The sensitivity is rather small steady during the time variation. It means that the resistance sensitivity small changes do not varies in time domain and are similar during the rise time and steady state time. The differences in the curves presented in Fig. 5 can be result of the method of calculating (10) is high resistance value dependent.

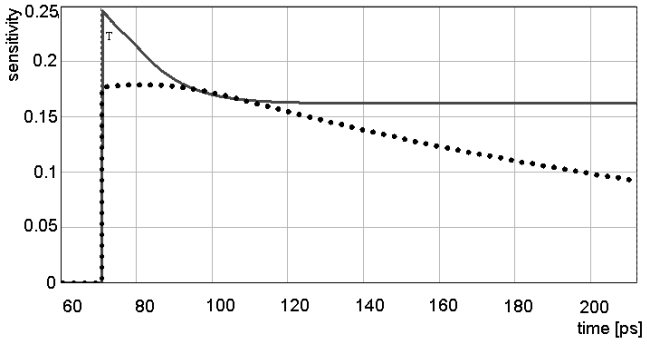

Fig. 5. Sensitivity of the ramp response to the resistance vs. time function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (10)

The sensitivity of the input gate output resistance is almost steady during the time varies and is about 0.25. The simulation result is presented in Fig. 6

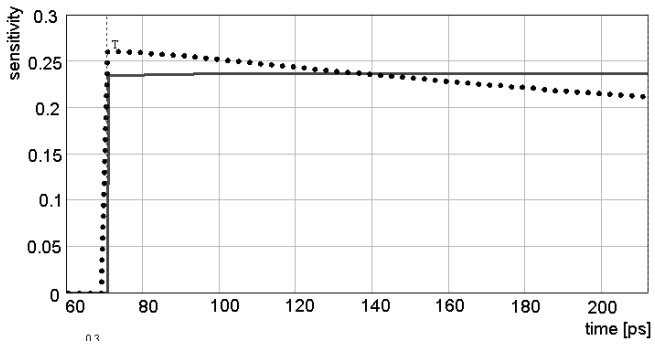

Fig. 6. Sensitivity of the ramp response to the resistance of the input gate vs. time function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (10)

The next simulation presents the sensitivity of the ramp response to the output gate input capacitance in time function (Fig.7.). The behavior is similar than when the line capacitance analyzing, but the sensitivity has smaller values (less than 1). For the threshold higher than 50% the sensitivity is smaller than 0.6.

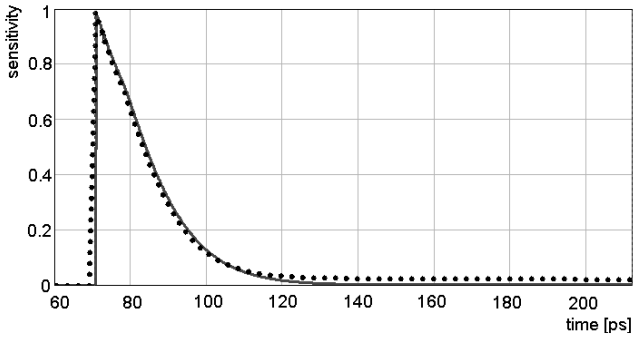

Fig. 7. Sensitivity of the ramp response to the output gate input capacitance vs. time function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (10)

The last simulation presents the sensitivity to different parameters (C_0, R_s, R) for the calculated from (12) formula for threshold time calculation. The obtained results shows that the closed form formula is more sensitive to the parameter changes than SPICE simulations, but the sensitivity is not high (Fig 8, Fig 9, Fig 10) compared to the ramp response sensitivity for the time of the 50% threshold.

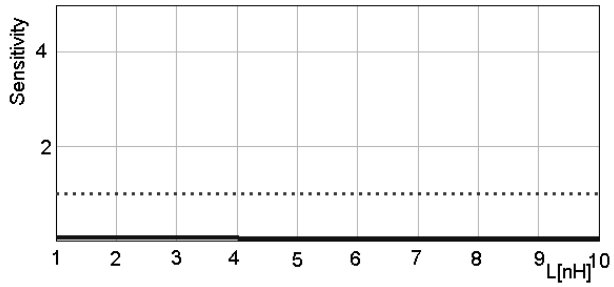

Fig. 8. Sensitivity of the threshold time (50% steady state) to the output gate input capacitance vs. inductance of the line function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (11)

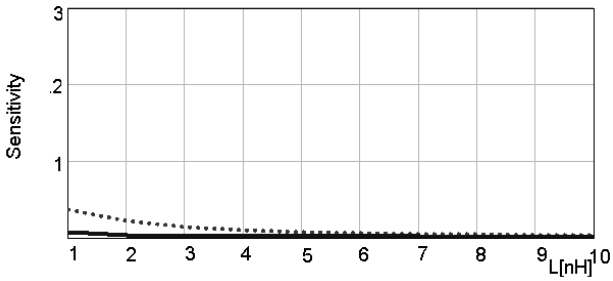

Fig. 9. Sensitivity of the threshold time (50% steady state) to the input gate output resistance Rs vs. inductance of the line function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (11)

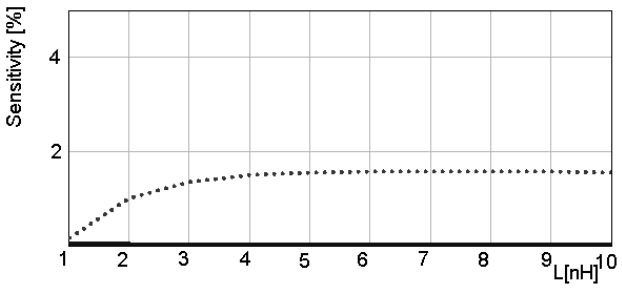

Fig. 10. Sensitivity of the threshold time (50% steady state) to the line resistance in inductance vs. the line function, the solid line presents the sensitivity from Spice simulation, the dots line presents formula (11)

IV. CONCLUSIONS

In the paper we present the sensitivity analysis for the ramp response of the interconnect and compare the results with the sensitivity of closed form formula (10) for the ramp response calculated with multiple scales method. The analysis is done in time domain. The analysis shows, that the presented approach has similar sensitivity to the interconnect parameter (L, C, C_0, R_w) variation, calculated from formula (10) to SPICE simulations sensitivity (12), (13). Changes in R parameter gives some differences in sensitivity analysis for SPICE and (10). The simulation shows that for wide range of typical low-loss interconnects the most important in perspective of sensitivity is rise time especially when the first traveling wave reaches the end of the interconnect. the presented approach allows to approve, that the formula for the ramp response (10) calculation presented above is valid for typical low-loss interconnects.

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